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| Results of search set L3: | et L3: | | |
| US 6754862 B1 US 6754633 B1 | Gaining access to internal nodes in a PLD Encoding a code signal into an audio or video signal | 20040622 714/725 20040622 704/273 | |
| US 6704889 B2 | Enhanced embedded logic analyzer System and method for translating a report file of one logic device to a constraints | 20040309 714/39 ; | |
| US 6536017 B1 US 6353921 B1 | file of another logic device Hardwire logic device emulating any of two or more FPGAs | 20030318 716/3 20020305 716/17 | |
| US 6226779 B1 | Programmable IC with gate array core and boundary scan capability | | |
| US 6134517 A US 6120551 A | Method of implementing a boundary scan chain Hardwire logic device emulating an FPGA | 20001017 703/28 20000919 716/17 | |
| US 6071314 A US 5991908 A | Programmable I/O cell with dual boundary scan Boundary scan chain with dedicated programmable routing | | |
| Results of search set L6: | et L6: | | |

US 6732068 B2

Memory circuit for use in hardware emulation system

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